

NTR09XXH3

(Covers NTR09RFH3, NTR09RSH3, NTR09CFH3, NTR09CSH3)

315MHz/+20dBm LoRa RF Transceiver Module

Datasheet

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Revision History

References

1. NTR09XXH3 315MHz/+20dBm LoRa RF Transceiver Module in Brief

NTR09XXH3 is a small size, compact, low power and easy to use 315MHz LoRa RF Transceiver module based on Semtech SX1262 Sub-GHz RF Transceiver IC. It supports both LoRa and G(FSK) modulations, provides radio configuration and control via the SPI interface and has up to -146dBm RF receiver sensitivity and up to +20dBm RF output power.

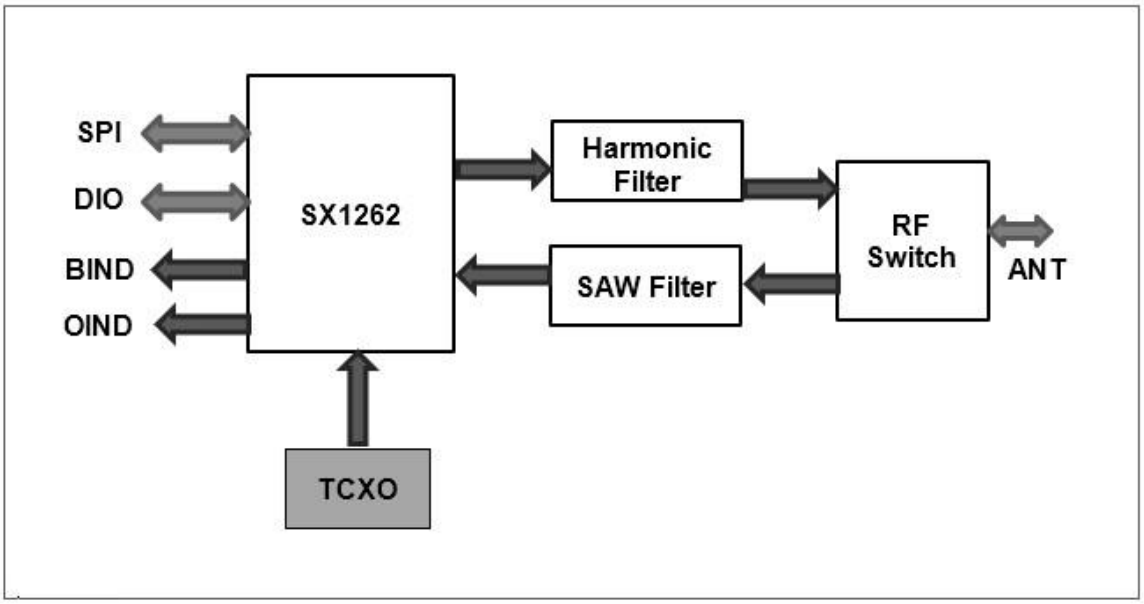


Fig.1 NTR09XXH3 functional blocks and interconnections

Features

- Wide supply voltage range, 1.8V~3.6V
- Operating frequency 315MHz with LoRa and (G)FSK modems
- Up to 62.5kbps bit rate for LoRa and up to 300kps bit rate for (G)FSK
- Packet mode with data buffer, data whitening codec, FEC-Forward Error Correction
- -146dBm Receiver sensitivity, (@SF12 and LoRa BW-10.4kHz)
- +20dBm RF output power (programmable with 1dB steps)
- High frequency stability, long range and high performance with TCXO
- Low power consumption,
    - 4.6mA, sleep mode <600nA (in receive mode)
    - 99mA (in transmit mode,@20dBm)
- Radio configuration and control via SPI interface
- Fully programmable frequency, modem, packet parameters and radio operational modes
- Small Size
    - NTR09RFH3 and NTR09RSH3 – 43.10mmx28.60mm
    - NTR09CFH3 and NTR09CSH3 – 38.90mmx28.60mm

Application Areas

- Low-cost consumer electronics applications, ISM band data communication
- Smart Building Automation
- Industrial Monitoring and Control
- Remote Control, Remote Keyless Entry, Remote AMR, Tag Reader
- Wireless Alarm and Security, Wireless Sensor Node

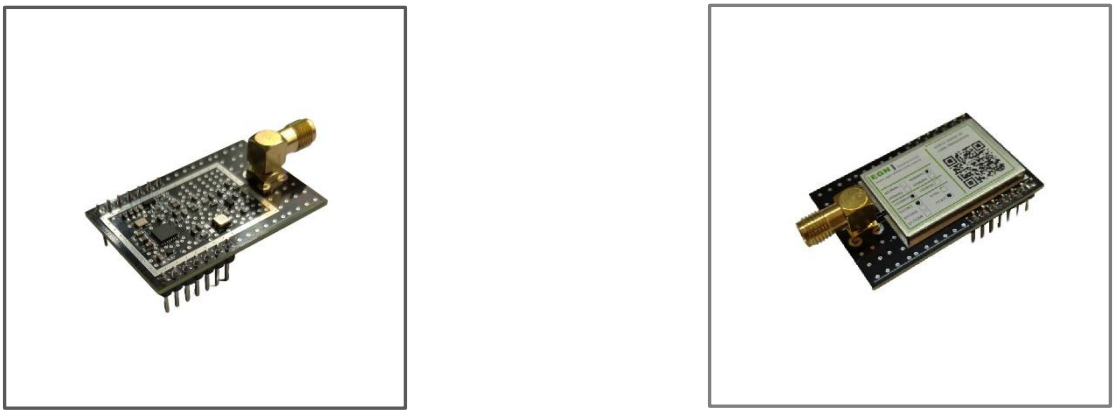


Fig.2 NTR09RFH3 (left) and NTR09RSH3 (right)

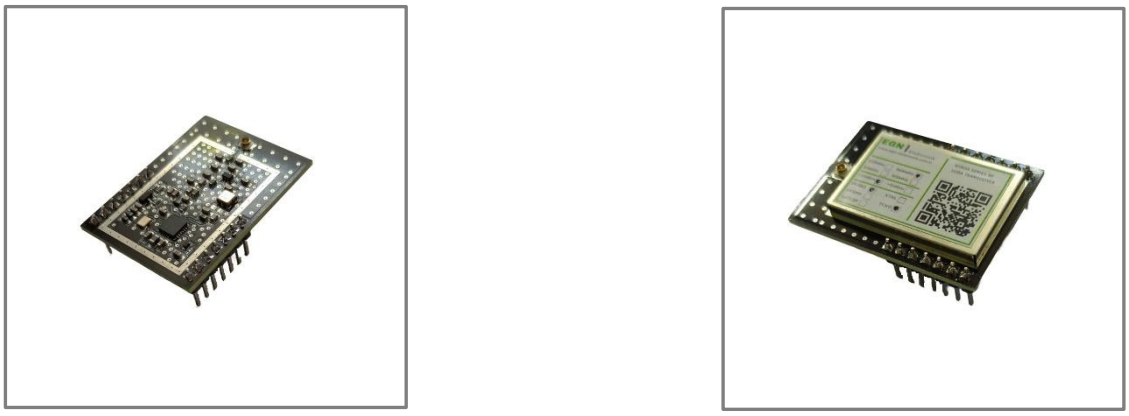


Fig.3 NTR09CFH3 (left) and NTR09CSH3 (right)

LoRa Modulation Technique

The NTR09XXH3 uses Semtech's patented LoRa modulation technique which combines spread spectrum modulation and forward error correction techniques to increase the range and robustness of radio communication links compared with traditional FSK or OOK based modulation. This high sensitivity, in contrast to conventional modulation techniques, permits an increase in link budget and increased immunity to in-band interference, combined with +20dBm RF power output yields industry leading link budget.

LoRa also provides significant advantages in both blocking and selectivity, solving the traditional design compromise between range, interference immunity and energy consumption. In LoRa mode the NTR09XXH3 offers ten bandwidth options as in table below.

Signal Bandwidth	0	1	2	3	4	5	6	7	8	9
BW_L (kHz)	7.81	10.42	15.63	20.83	31.25	41.67	62.5	125	250	500

Table 1. NTR09XXH3 LoRa Mode BW Options

The spread spectrum LoRa modulation is performed by representing each bit of payload information by multiple chips of information. The rate at which the spread information is sent is referred to as the symbol rate (Rs), the ratio between the nominal symbol rate and chip rate is the spreading factor and represents the number of symbols sent per bit of information. The range of parameters which can be configured are given in the following tables.

Spreading Factor (SF)	5	6	7	8	9	10	11	12
Chips/Symbol	32	64	128	256	512	1024	2048	4096
SNR (dB)	-2.5	-5.0	-7.5	-10.0	-12.5	-15.0	-17.5	-20.0

Table 2. NTR09XXH3 LoRa Mode Spreading Factors

Note that the spreading factor must be known in advance on both transmit and receive sides of the radio link as different spreading factors are orthogonal to each other. Note also the resulting signal to noise ratio (SNR) required at the receiver input. It is the capability to receive signals with negative SNR that increases the sensitivity, so link budget and range, of the LoRa receiver.

To further improve the robustness of the radio link NTR09XXH3 provides cyclic error coding with different coding rates. By using this coding scheme forward error detection and correction can be applied.

Differentiating Aspects of The NTR09XXH3 315MHz LoRa RF Transceiver Module

Main performance contributors of NTR09XXH3 are use of TCXO for high frequency stability and precision, use of harmonic filters for transmitter harmonic suppression and use of 315MHz SAW filter in RX path providing high selectivity which consequently providing high interference immunity and high sensitivity resulting in long range and exceptional bit error rate performance even in highly interfering environments with low SNR/SINR values. TCXO and SAW filter characteristics are given below.

NTR09XXH3 is optimized for +20dBm RF power output, PA settings should be arranged according to Section 5. Setting Modem, Transmitter & Receiver Parameters as in Table12B, for other PA configuration settings matching is not optimum and the RF power output may be different from intended usually at a higher current consumption.

32MHz TCXO - (Temperature Compensated Crystal Oscillator) for High Accuracy and Stability

Under certain circumstances, like in environments with extreme temperature variation, it is usually required to use a TCXO (Temperature Compensated Crystal Oscillator) to achieve better frequency accuracy. This depends on the complete system, transmitter and receiver and especially for LoRa modulation maximum tolerated frequency drifts for different data rates can be found in SX1262 Datasheet. When using the LoRa modulation with *LowDataRateOptimize* set to 0x00, the total frequency drift over the packet transmission time should be minimized and kept lower than *Freq_drift_max*:

For high accuracy, stability, long range communication link reliability and robustness NTR09XXH3 uses TCXO instead of XTAL, TCXO use specific settings are detailed in Section 6. Module Aspects To Consider for User Application

315MHz SAW Filter for High Selectivity and Interference Immunity

NTR09XXH3 includes a highly selective 315MHz SAW filter in RF frontend in RX path for additional interference suppression. The characteristics of the SAW filter are given in Table 3 and Fig 4 below.

Parameter	Test Conditions	Min	Typical	Max	Unit
Center Frequency		-	315	-	MHz
3-dB Bandwidth		-	4	-	MHz
Attenuation	293 to 293.9MHz	53	58		dB
	304 to 304.6MHz	48	53		
	325.4 to 326MHz	24	31		
	336.1 to 337MHz	36	41		

Table 3. NTR09XXH3 SAW Filter Characteristics

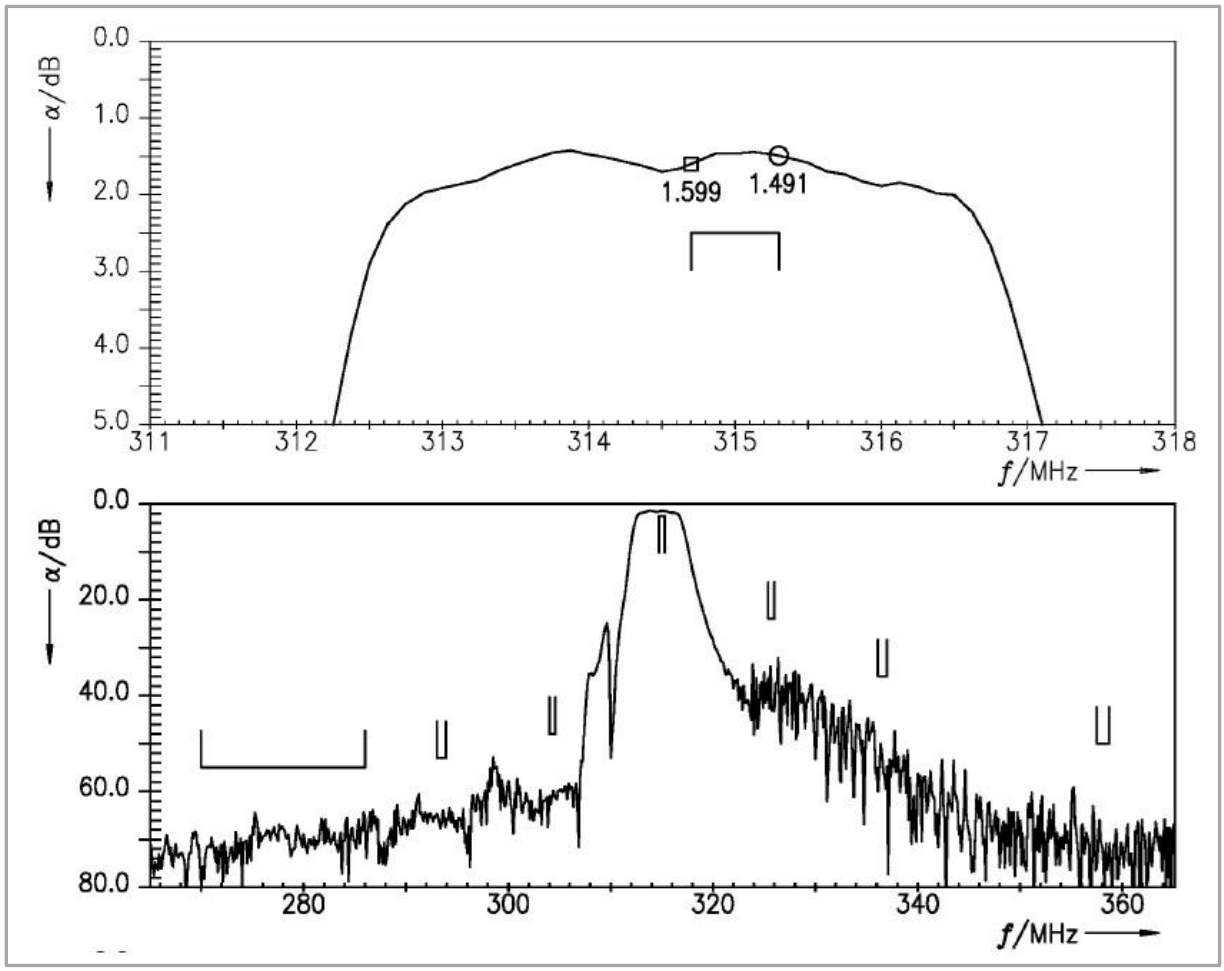


Fig.3 NTR09XXH3 RF Frontend SAW Filter Frequency Response

Due to highly selective SAW filter use, severe performance degradations might be expected when operating frequency selected does not fit inside filter BW, therefore for optimal receiver performance an operating frequency in 313MHz-316.5MHz range should be selected.

2. NTR09XXH3 Technical Data

The tables below give the electrical specifications for the NTR09XXH3 315MHz LoRa RF Transceiver Module operating with LoRa and FSK/(G)FSK modulation.

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
F_{op}	Operational Frequency/Band	-	-	315	-	MHz
$S_{RFIN-FSK}$	Sensitivity-FSK	@4.8kbps, BW-20kHz	-	-117	-	dBm
		@0.6kbps, BW-4kHz	-	-122		
$S_{RFIN-LoRa}$	Sensitivity-LoRa	@SF12, BW-10.4kHz	-	-146	-	dBm
		@SF7, BW-500kHz	-	-116	-	
CCR_{FSK}	Co-channel Rejection-FSK			-9		dB
CCR_{LoRa}	Co-channel Rejection-LoRa	@SF12		19		dB
ACR_{FSK}	Adjacent-channel Rejection-FSK	+/-50kHz offset		45		dB
ACR_{LoRa}	Adjacent-channel Rejection-LoRa	+/-187kHz offset,SF-12		72		dB
BI_{FSK}	Blocking Immunity-FSK (4.8kbps, BW-20kHz)	+/-1MHz offset		68		dB
		+/-2MHz offset		70		
		+/-10MHz offset		80		
BI_{LoRa}	Blocking Immunity-LoRa (SF12, BW-125kHz)	+/-1MHz offset		88		dB
		+/-2MHz offset		90		
		+/-10MHz offset		99		
IMA	Image Attenuation-LoRa	with IQ calibration		54		dB
IIP_3	Third Order Intercept Point	Two tone test (1MHz/1.96MHz)	-	-5	-	dBm

Table 4. RF Radio Receiver /Receive Mode Characteristics

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
F_{op}	Operational Frequency/Band	-	-	315	-	MHz
P_{RFOUT}	Maximum Output Power	-	-	+20	-	dBm
P_{RF-sat}	Power Change Step Size	Programmable	-	1	-	dB
P_{STEP}	RF Output Power Range	Programmable	-11	-	+20	dBm
P_{RMP}	RF Output Power Ramping Time	Programmable	10	-	3400	usec

Table 5. RF Radio Transmitter/Transmit Mode Characteristics

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
F_{step}	Synthesizer Frequency Step Size	-	-	0.95	-	Hz
SF_{LoRa}	Spreading Factor-LoRa	Programmable	5	-	12	-
BR_{LoRa}	Bit Rate-LoRa	Programmable	0.018	-	62.5	kbps
BW_{LoRa}	Bandwidth-LoRa	Programmable	7.8		500	kHz
BR_{FSK}	Bit Rate-FSK	Programmable	0.6	-	300	kbps
FDA_{FSK}	Frequency Deviation-FSK	Programmable	0.6	-	200	kHz

Table 6. LoRa/FSK Modem and Frequency Synthesizer Characteristics

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
V_{IH}	Input High Voltage		0.7*VCC	-	VCC+0.3	V
V_{IL}	Input Low Voltage		-0.3	-	0.3*VCC	V
V_{OH}	Output High Voltage		0.9*VCC	-	VCC	V
V_{OL}	Output Low Voltage		0	-	0.1*VCC	V
V_{IL_NRST}	Input High Voltage for NRST		-0.3	-	0.2*VCC	V

Table 7. Digital I/O Characteristics

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
V_{cc}	Supply Voltage	-	1.8	3.3	3.6	V
I_{dd_SLP}	Current–Sleep mode		-	600	-	nA
I_{dd_TX}	Current–Transmit mode		-	99	-	mA
I_{dd_RX}	Current–Receive mode		-	4.6	-	mA
T_{op}	Operational Temperature	-	-40	-	+85	ºC

Table 8. Electrical Specifications

Absolute Maximum Ratings

"Absolute maximum ratings" may cause permanent damage to the device and is a stress rating only, functional operation of the device under these conditions for extended periods may affect device reliability.

Symbol	Parameter	Max	Unit
VDD	Supply voltage	3.6	V
T_{op}	Operational Temperature	-40~+85	ºC
T_{stg}	Storage Temperature	-50~+150	ºC
ESD	ESD Rating	2(HBM)	kV

Table 9. Absolute Maximum Ratings

3. Interfacing NTR09XXH3 to Host Controller

The NTR09XXH3 is controlled via a serial SPI interface and a general-purpose input/output (DIO1) used for IRQ. The BIND (Busy Indicator) line is mandatory to ensure the host controller is ready to accept the commands. BIND is used as a busy signal indicating that the module is ready for new command only if this signal is low. When BIND is high, the host controller must wait until it goes down again before sending another command. Through SPI the application sends commands to the internal chip or accesses directly the data memory space.

Reset

A complete "factory reset" of the SX1262 in module can be issued on request by toggling pin NRST of the NTR09XXH3. It will be automatically followed by the standard calibration procedure and any previous context will be lost. The pin should be held low for more typically 100µs for the Reset to happen.

SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL= 0 and CPHA = 0 and NTR09XXH3 behaves as slave. An address byte followed by a data byte is sent for a write access whereas an address byte is sent, and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte. MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK. A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high. The SPI runs on the external SCK clock provided by the master.

SPI Timing When the Transceiver Leaves Sleep Mode

In Sleep mode and during the initialization phase, the busy signal mapped on BIND pin, is set high indicating to the host that the module is not able to accept a new command. Once the module is in STDBY_RC mode, the busy signal goes low, and the host can start sending a command. This is also true for startup at battery insertion or after a hard reset.

One way for the module to leave Sleep mode is to wait for a falling edge of NSS. At falling edge, all necessary internal regulators are switched On; the module starts initialization before being able to accept first SPI command. This means that the delay between the falling edge of NSS and the first rising edge of SCK must take into account the wake-up sequence and the initialization.

Through the SPI interface, the host can issue commands to the module or access the data memory space to directly retrieve or write data. In normal operation, a reduced number of direct data write operations is required except when accessing the data buffer.The user interacts with the circuit through an API (instruction set).

The NTR09XXH3 module BIND pin indicates the status of the module and its ability (or not) to receive another command while internal processing occurs. Prior to executing one of the generic functions, it is thus necessary to check the status of BIND to make sure the module is in a state where it can process another function.

Command Structure

In case of a command that does not require any parameter, the host sends only the opcode (1 byte). In case of a command which requires one or several parameters, the opcode byte is followed immediately by parameter bytes with the NSS rising edge terminating the command.

Transaction Termination

The host terminates an SPI transaction with the rising NSS signal; the host does not explicitly send the command length as a parameter. The host must not raise NSS within the bytes of a transaction. If a transaction sends a command requiring parameters, all the parameters must be sent before rising NSS, if not the module will take some unknown value for the missing parameters.

More details about SPI interface, command structures, registers and FIFO can be found in SX1262 Datasheet.

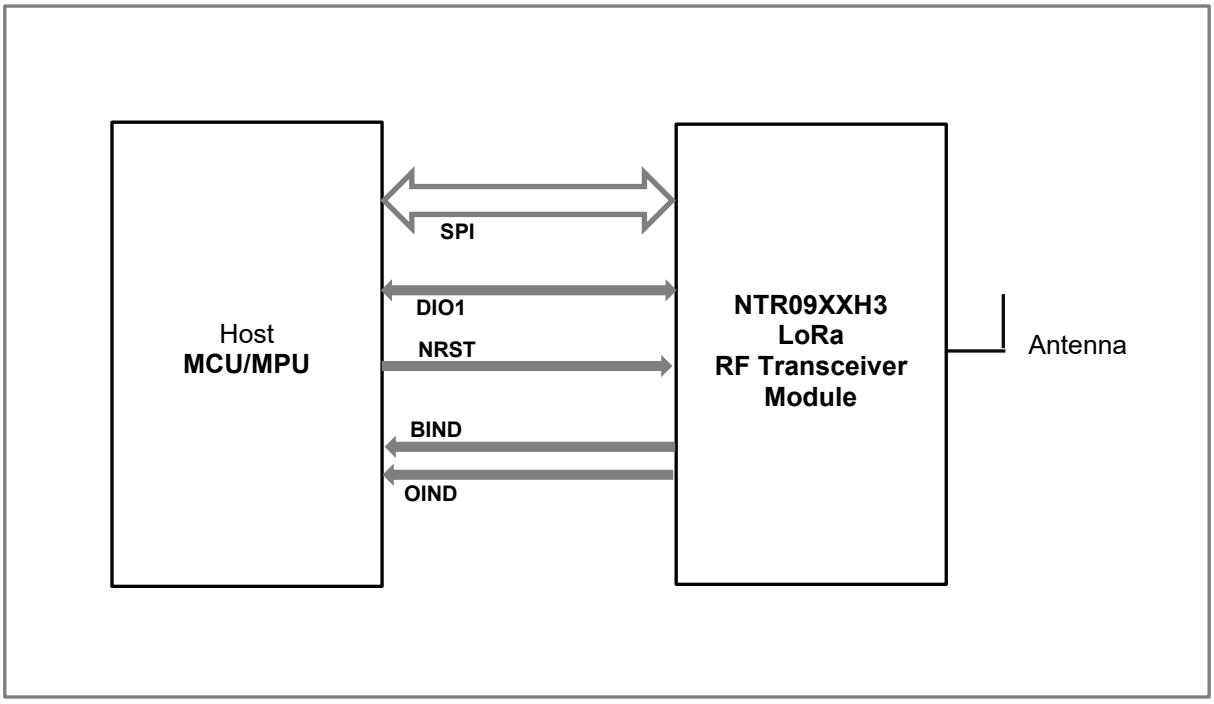


Fig.5 Interfacing NTR09XXH3 to MCU/MPU

4. Operational Modes

The NTR09XXH3 features six operating modes based on operating modes of SX1262, each operating mode is explained in the following table and details of operational modes can be found in SX1262 Datasheet.

Operation Mode	Enabled Blocks
SLEEP	Optional registers, backup regulator, RC64k oscillator, data RAM
STANDBY_RC	Top regulator (LDO), RC13M oscillator
STANDBY_XOSC	Top regulator (DC-DC or LDO), XOSC
FS	All of the above + Frequency synthesizer at Tx frequency
TX	Frequency synthesizer and transmitter, Modem
RX	Frequency synthesizer and receiver, Modem

Table 10. NTR09XXH3 Operational Modes

Startup

At power-up or after a reset, the module goes into STARTUP state, the control being done by the sleep state machine operating at the battery voltage. The BIND pin is set to high indicating that the module is busy and cannot accept a command. When the digital voltage and RC clock become available, SX1262 can boot up and the CPU takes control. At this stage the BIND line goes down and the device is ready to accept commands.

Calibration

The calibration procedure is automatically called in case of POR or via the calibration command. Parameters can be added to the calibrate command to identify which section of calibration should be repeated. The following blocks can be calibrated:

• RC64k using the 32 MHz TCXO as reference
• RC13M using the 32 MHz TCXO as reference
• PLL to select the proper VCO frequency and division ratio for any RF frequency
• RX ADC
• Image (RX mode with defined tone)

Once the calibration is finished, the chip enters STDBY_RC mode.

Sleep Mode

In this mode, most of the radio internal blocks are powered down or in low power mode and optionally the RC64k clock and the timer are running. The chip may enter this mode from STDBY_RC and can leave the SLEEP mode if one of the following events occurs:

• NSS pin goes low in any case
• RTC timer generates an End-Of-Count (corresponding to Listen mode)

When the radio is in Sleep mode, the BIND pin is held high.

Standby (STDBY) Mode

In standby mode the host should configure the module before going to RX or TX modes. By default in this state, the system is clocked by the 13 MHz RC oscillator to reduce power consumption (in all other modes except SLEEP the XTAL is turned ON).

However, if the application is time critical, the XOSC block can be turned or left ON. XOSC or RC13M selection in standby mode is determined by mode parameter in the command *SetStandby(...)*.

The mode where only RC13M is used is called STDBY_RC and the one with XOSC ON is called STDBY_XOSC.

Frequency Synthesis (FS) Mode

In FS mode, PLL and related regulators are switched ON. The BIND goes low as soon as the PLL is locked or timed out. For debugging purposes the chip may be requested to remain in this mode by using the *SetFs()* command

Receive (RX) Mode

In RX mode, the RF front-end, RX ADC and the selected modem (LoRa or FSK) are turned ON. In RX mode the circuit can operate in different sub-modes:

• Continuous mode: the device remains in RX mode and waits for incoming packet reception until the host requests a different mode,
• Single mode: the device returns automatically to STDBY_RC mode after packet reception,
• Single mode with timeout: the device returns automatically to STDBY_RC mode after packet reception or after the selected timeout,
• Listen mode: the device alternate between Sleep and Rx mode until an IRQ is triggered.

In RX mode, BIND will go low as soon as the RX is enabled and ready to receive data.

The NTR09XXH3 can operate in Rx Boosted gain setup or in Rx power saving gain setup. In the Rx power saving gain, the radio will consume less power at a small cost in sensitivity. In Rx Boosted gain, the radio will consume more power to improve the sensitivity.

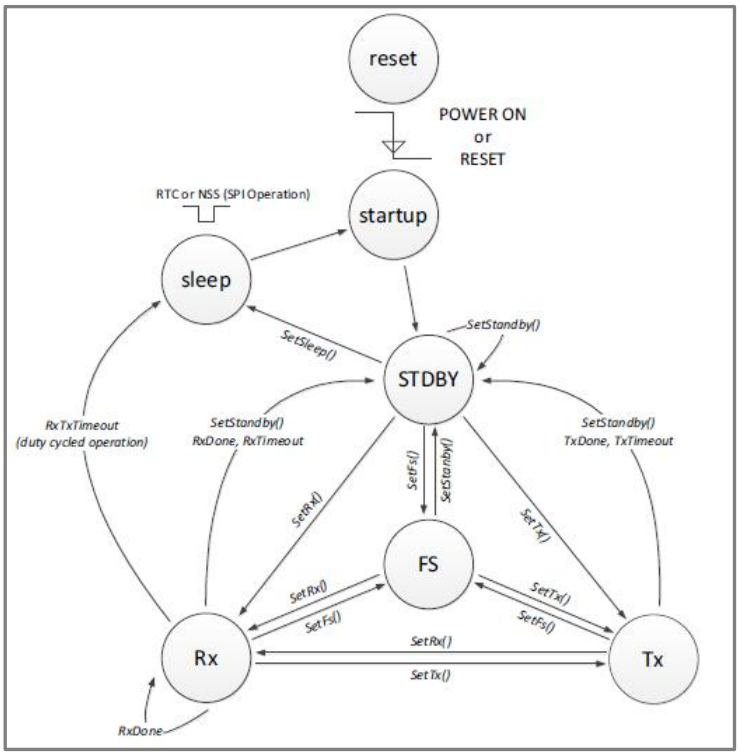


Fig.6 NTR09XXH3 Operational Modes

Transmit (TX) Mode

In TX mode, after enabling and ramping-up the Power Amplifier (PA), the contents of the data buffer are transmitted. The circuit can operate in different sub-modes: single mode or single with timeout mode.

In TX mode, BIND will go low as soon as the PA has ramped-up and transmission of preamble starts.

PA Ramping

The ramping of the PA can be selected while setting the output power by using the command *SetTxParams(...)*. The PA ramp time can be selected to go from 10us up to 3.4ms.

5. Setting Modem, Transmitter & Receiver Parameters

The SX1262 and consequently NTR09XXH3 contains different modems capable of handling LoRa and FSK modulations. LoRa and FSK are associated with their own frame and modem.

The user specifies the modem and frame type by using the command *SetPacketType(...)*. This command specifies the frame used and consequently the modem implemented. This function is the first one to be called before going to Rx or Tx and before defining frequency, modulation and packet parameters.

LoRa Modulation Technique and LoRa Parameters

The LoRa modem uses spread spectrum modulation and forward error correction techniques to increase the range and robustness of radio communication links compared to traditional FSK based modulation. An important facet of the LoRa modem is its increased immunity to interference. The LoRa modem is capable of co-channel GMSK rejection of up to 19 dB. This immunity to interference permits the simple coexistence of LoRa modulated systems either in bands of heavy spectral usage or in hybrid communication networks that use LoRa to extend range when legacy modulation schemes fail.

Modulation Parameter

It is possible to optimize the LoRa modulation for a given application, access is given to the designer to four critical design parameters, each one permitting a trade-off between the link budget, immunity to interference, spectral occupancy and nominal data rate. These parameters are:

• Modulation BandWidth (BW_L)
• Spreading Factor (SF)
• Coding Rate (CR)
• Low Data Rate Optimization (LDRO)

These parameters are set using the command *SetModulationParams(...)* which must be called after *SetPacketType(...).*

LoRa has its own packet engine that supports the LoRa PHY. More details about LoRa Modem, LoRa Modulation Paramaters, LoRa Packet Engine, LoRa Frame and LoRa Channel Activity Detection (CAD) can be found in SX1262 Datasheet.

FSK/(G)FSK Modulation Technique and FSK/(G)FSK Parameters

The FSK modem can perform transmission and reception of 2-FSK modulated packets over a range of data rates from 0.6 kbps to 300 kbps. All parameters are set by using the command *SetModulationParams(...)*. This function should be called only after defining the protocol. The bitrate setting is referenced to the crystal oscillator and provides a precise means of setting the bit rate (or equivalently chip) rate of the radio.

The SX1262 and consequently NTR09XXH3 is designed for packet-based transmission. The packet controller block is responsible for assembly of the received data bit-stream into packets and their storage into the data buffer. It also performs the bit-stream decoding operations such as de-whitening & CRC-checks on the received bit-stream. On the transmit side, the packet handler can construct a packet and send it bit by bit to the modulator for transmission. It can whiten the payload and append the CRC-checksum to the end of the packet. The packet controller only works in half-duplex mode i.e. either in transmit or receive at a time. The packet controller is configured using the command *SetPacketParams(...)*

More details about FSK Modem, FSK Modulation Parameters, FSK Packet Format, FSK Frame and CRC use in FSK can be found in SX1262 Datasheet.

RF Frequency, PA and TX Parameters

RF Frequency Setting

The command *SetRfFrequency(...)* is used to set the frequency of the RF frequency mode. The LSB of Freq is equal to the PLL step giving:

$$RFfrequency = \frac{RFFreqxFXTAL}{2^{25}}$$

SetRfFrequency(...) defines the chip frequency in FS, TX and RX modes. In RX, the frequency is internally lowered to IF (250kHz by default).

Byte	0	1-4
Data from Host	Opcode=0x86	RFfreq(31:0)

Table 11. RF Frequency Setting

RF Frequency	RFfreq(31:0)
315MHz	0x13B00000
312MHz	0x13800000
314MHz	0x13A00000
316MHz	0x13C00000
318MHz	0x13E00000

Table 11B. NTR09XXH3 Typical Frequency Settings

PA Configuration

NTR09XXH3 PA matching hardware is optimal for +20dBm output power, therefore a sample set of PA settings are provided here.

paDutyCycle controls the duty cycle (conduction angle). The maximum output power, the power consumption, and the harmonics will drastically change with *paDutyCycle*. Changing the *paDutyCycle* will affect the distribution of the power in the harmonics and should be selected to work in conjunction with a given matching network. For implemented matching network, *paDutyCycle* can be selected as 0x04.

hpMax selects the size of the PA. The maximum output power can be reduced by reducing the value of *hpMax*. For implemented matching network, *hpMax* can be selected as 0x06.

deviceSel is reserved and has always the value 0x00.

paLut is reserved and has always the value 0x01.

PA Optimal Settings

Byte	0	1	2	3	4
Data from Host	Opcode=0x98	paDutyCycle	hpMax	deviceSel	paLut

Table 12. PA Settings

Byte	0	1	2	3	4
Data from Host	Opcode=0x98	0x04	0x06	0x00	0x01

Table 12B. NTR09XXH3 Recommended PA Settings

TX Parameters

SetTxParams command sets the TX output power by using the parameter *power* and the TX ramping time by using the parameter *RampTime.*

The power ramp time is defined by the parameter *RampTime* as defined in the following table

Byte	0	1	2
Data from Host	Opcode=0x8E	power	RampTime

Table 13. TX Settings

Byte	0	1	2
Data from Host	Opcode=0x8E	0x16	0x00

Table 13B. NTR09XXH3 Recommended TX Settings

RampTime	Value	RampTime(us)
SET_RAMP_10U	0x00	10
SET_RAMP_20U	0x01	20
SET_RAMP_40U	0x02	40
SET_RAMP_80U	0x03	80
SET_RAMP_200U	0x04	200
SET_RAMP_800U	0x05	800
SET_RAMP_1700U	0x06	1700
SET_RAMP_3400U	0x07	3400

Table 14. PA Ramp Time Settings

Data Buffer

The transceiver is equipped with a 256-byte RAM data buffer which is accessible in all modes except sleep mode. This RAM area is fully customizable by the user and allows access to either data for transmission or from the last packet reception.

Data Buffer in Receive Mode

In receive mode *RxBaseAddr* specifies the buffer offset in memory at which the received packet payload data will be written. The buffer offset of the last byte written in receive mode is then stored in *RxDataPointer* which is initialized to the value of *RxBaseAddr* at the beginning of the reception.

The pointer to the first byte of the last packet received and the packet length can be read with the command *GetRxbufferStatus().* In single mode, *RxDataPointer* is automatically initialized to *RxBaseAddr* each time the transceiver enters Rx mode. In continuous mode the pointer is incremented starting from the previous position.

Data Buffer in Transmit Mode

Upon each transition to transmit mode *TxDataPointer* is initialized to *TxBaseAddr* and is incremented each time a byte is sent over the air. This operation stops once the number of bytes sent equals the payloadlength parameter as defined in the function *SetPacketParams(...).*

Using the Data Buffer

Both, *RxBaseAddr* and *TxBaseAddr* are set using the command *SetBufferBaseAddresses(...).* By default *RxBaseAddr* and *TxBaseAddr* are initialized at address 0x00.

Due to the contiguous nature of the data buffer, the base addresses for Tx and Rx are fully configurable across the 256-byte memory area. Each pointer can be set independently anywhere within the buffer. To exploit the maximum data buffer size in transmit or receive mode, the whole data buffer can be used in each mode by setting the base addresses *TxBaseAddr* and *RxBaseAddr* at the bottom of the memory (0x00).

The data buffer is cleared when the device is put into Sleep mode (implying no access). The data is retained in all other modes of operation.

Note:
All the received data will be written to the data buffer even if the CRC is invalid, permitting user-defined post processing of corrupted data. When receiving, if the packet size exceeds the buffer memory allocated for the Rx, it will overwrite the transmit portion of the data buffer.

More details about Data Buffer, Use of Data Buffer, Writing to and Reading from Buffer and Registers can be found in SX1262 Datasheet.

6. Module Aspects To Consider for User Application

NTR09XXH3 315MHz LoRa RF Transceiver module is capable of using LDO Only or LDO+DC-DC mode of operation, uses TCXO for high frequency stability and also uses an RF switch for TX and RX path switching in transmit and receive modes respectively. The user application code should contain proper settings for LDO Only or LDO+DC-DC mode of operation, TCXO use, RF switch use and proper calibration as detailed in following sections.

LDO Only or LDO plus DC-DC Mode of Operation

In SX1262 two forms of voltage regulation (DC-DC buck converter or linear LDO regulator) are available, the linear LDO regulator is always present in all modes but the transceiver will use DC-DC when selected. By default, only the LDO is used. *SetRegulatorMode(...)* function specifies if DC-DC or LDO is used for power regulation. The user can specify the use of DC-DC by using the command *SetRegulatorMode(...)*. This operation must be carried out in STDBY_RC mode only. The regulation mode is defined by parameter *regModeParam*.

Byte	0	1
Data from Host	Opcode=0x96	regModeParam 0: Only LDO used for all modes 1: DC_DC+LDO for STBY_XOSC,FS, RX and TX

Table 15. Regulator Mode Selection

Hardware implementation of the NTR09XXH3 allows using LDO only or LDO plus DC-DC mode of operations.

TCXO for High Frequency Stability (Controlled by DIO3)

NTR09XXH3 uses TCXO which is automatically power cycled by DIO3 multifunction I/O pin of SX1262, therefore the user application should take use of TCXO into account detailed as follows. DIO3 of SX1262 needs to be configured to automatically control the 32MHz TCXO through the command *SetDio3AsTCXOCtrl(...)*.

Byte	0	1	2-4
Data from Host	Opcode=0x97	tcxoVoltage	delay(23:0)

Table 16. TCXO Control by DIO3

When this command is used, the SX1262 now controls the TCXO itself through DIO3. In STDBY_XOSC, FS, TX and RX modes, the internal state machine will set DIO3 to a predefined output voltage defined by the parameter *tcxoVoltage*.

tcxoVoltage	Description
0x00	DIO3 outputs 1.6V to supply the TCXO
0x01	DIO3 outputs 1.7V to supply the TCXO
0x02	DIO3 outputs 1.8V to supply the TCXO
0x03	DIO3 outputs 2.2V to supply the TCXO
0x04	DIO3 outputs 2.4V to supply the TCXO
0x05	DIO3 outputs 2.7V to supply the TCXO
0x06	DIO3 outputs 3.0V to supply the TCXO
0x07	DIO3 outputs 3.3V to supply the TCXO

Table 17. TCXO Control Voltage Settings

The time needed for the 32 MHz to appear and stabilize can be controlled through the parameter *delay(23:0)*. If the 32 MHz from the TCXO is not detected internally at the end of the delay period, the error XOSC_START_ERR will be flagged in the error controller. The timeout duration is defined by

$$Delay\ duration = Delay(23:0)*15.625\mu s$$

The TCXO will not be immediately ready at the desired frequency and will suffer from an initial setup time where the frequency is gently drifting toward the wanted frequency. This setup time is different from one TCXO to another, therefore, to ensure this setup time does not have any effect on the modulation or packets, the delay value will internally gate the 32 MHz coming from the TCXO to give enough time for this initial drift to stabilize. At the end of the delay period, the internal block will stop gating the clock and the radio will carry on to the next step.

Note: The user should take the delay period into account when going into Tx or Rx mode from STDBY_RC mode. Since the time needed to switch modes will increase with the duration of delay. To avoid increasing the switching mode time, the user can first set the device in STDBY_XOSC which will switch on the TCXO and wait for the delay period. Then, the user can set the device into Tx or Rx mode without suffering from any delay in addition to the internal processing.

Note:
A complete Reset of the chip is required to get back to normal XOSC operation, after the chip has been set to TCXO mode with the command *SetDIO3AsTCXOCtrl*.

Note:
The XOSC_START_ERR flag will be raised at POR or at wake-up from Sleep mode in a cold-start condition, when a TCXO is used. It is an expected behavior since the SX1262 is not yet aware of being clocked by a TCXO. The user should simply clear this flag with the *ClearDeviceErrors* command.

Note:
In case of POR or when the device is recovering from Sleep mode in cold start mode, the image calibration is performed as part of the initial calibration process and for optimal image rejection in the band 470MHz - 510MHz. When the 32 MHz clock is coming from a TCXO, the calibration will fail and the user should request a complete calibration after calling the function *SetDIO3AsTcxoCtrl(...).*

Note:

For proper operation of the NTR09XXH3, the DIO3 should be configured accordingly, tests are performed with *tcxoVoltage* value of 2.7V(0x05 in Hex) and *delay(23:0)* value of 4ms (0x0000FF in Hex).

Image Calibration for 315MHz Frequency Band

Image calibration is done through the command *CalibrateImage(...)* for a given range of frequencies defined by the parameters *freq1* and *freq2*. Once performed, the calibration is valid for all frequencies between the two extremes used as parameters. Typically, the user can select the parameters *freq1* and *freq2* to cover any specific ISM band.

Byte	0	1	2
Data from Host	Opcode=0x98	freq1	freq2

Table 18. Image Calibration for 315MHz frequency band

By default, the image calibration is made in the band 902MHz-928MHz, therefore it should be repeated by requesting the device to perform a new image calibration for 315MHz frequency band by defining 310MHz-320MHz band.

Frequency Band	freq1	freq2
310MHz-320MHz	0x4D	0x51

Table 19. Image Calibration Frequencies

Use of RF Switch (controlled by DIO2)

NTR09XXH3 uses an RF switch to activate/deactivate TX and RX paths in transmit and receive modes respectively, and RF switch used is controlled by DIO2 multifunction I/O pin of SX1262, therefore the user application should take use of DIO2 into account detailed as follows.

DIO2 should be configured to drive the RF switch through the use of the command *SetDio2AsRfSwitchCtrl(...)*. In this mode, DIO2 will be at a logical 1 during Tx and at a logical 0 in any other mode. DIO2 will be asserted high a few microseconds before the ramp-up of the PA and will be set to zero after the ramp-down of the PA.

Byte	0	1
Data from Host	Opcode=0x9D	enable

Table 20. DIO2 RF Switch Configuration

The enable byte definition is given as follows:

Enable	Description
0x00	DIO2 is free to be used as an IRQ
0x01	DIO2 is selected to be used to control an RF switch. In this case: DIO2 = 0 in SLEEP, STDBY_RX, STDBY_XOSC, FS and RX modes, DIO2 = 1 in TX mode

Table 21. DIO2 Options

Note:

For proper operation of the NTR09XXH3, the DIO2 should be configured accordingly by enabling with 0x01 parameter.

Application Code Structure and Issuing Commands in the Right Order

NTR09XXH3 hardware is suitable for LDO only operation, includes an RF switch controlled by DIO2 of SX1262 and a TCXO where the control voltage is supplied by DIO3 of SX1262, therefore related IRQ/DIO mask settings, TCXO settings and RF switch settings should be configured, transmit and receive buffer base addresses should be defined and a calibration should be performed before radio configuration and operation.

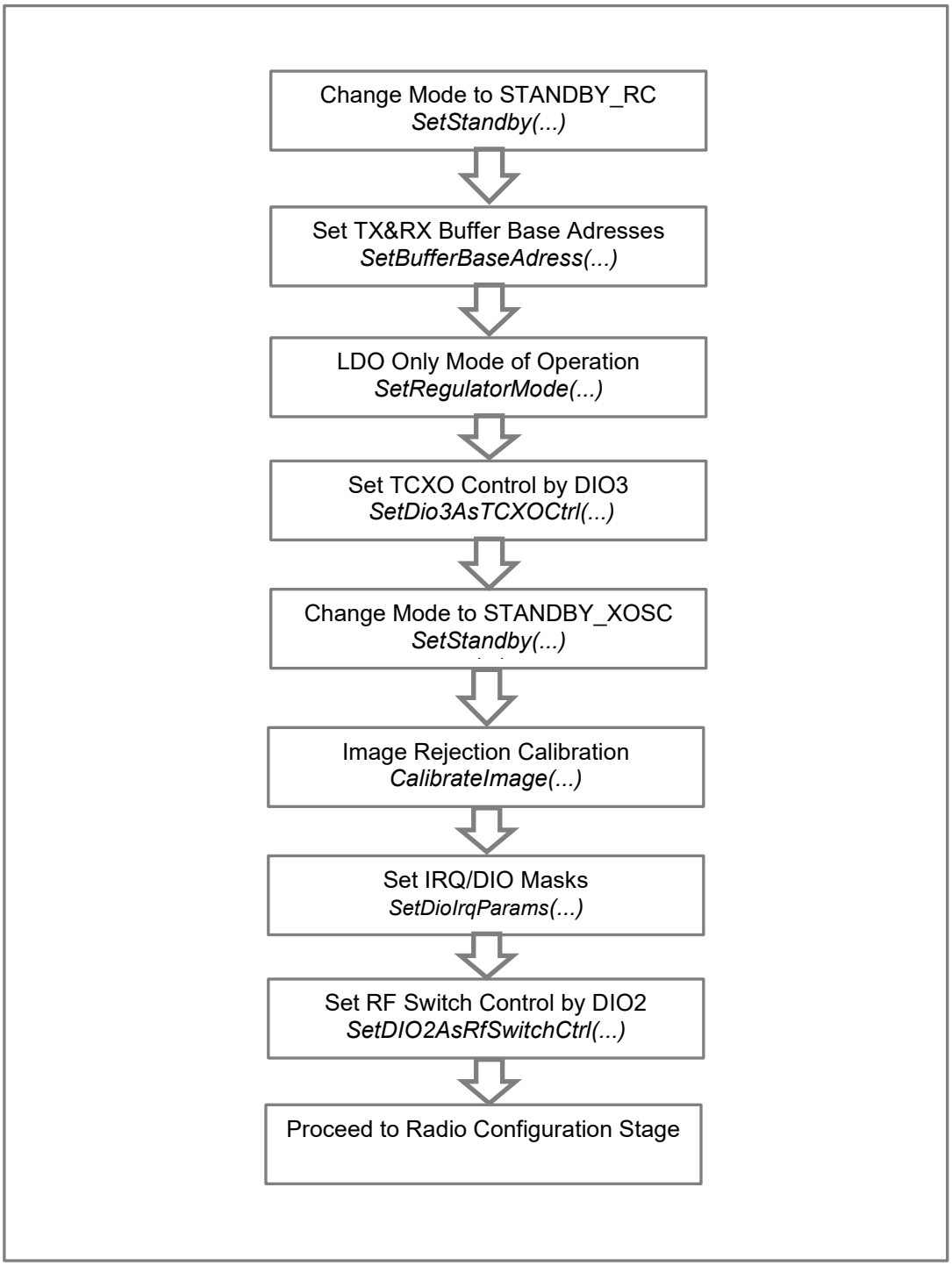


Fig.7 Configuration and Settings - Standby Mode

Most of the commands can be sent in any order except for the radio configuration commands which will set the radio in the proper operating mode.

It is mandatory to set the radio protocol using the command *SetPacketType(...)* as a first step before issuing any other radio configuration commands.

In a second step, the user should define the modulation parameter according to the chosen protocol with the command *SetModulationParams(...).*

Finally, the user should then select the packet format with the command *SetPacketParams(...).*

Note: If this order is not respected, the behavior of the device could be unexpected

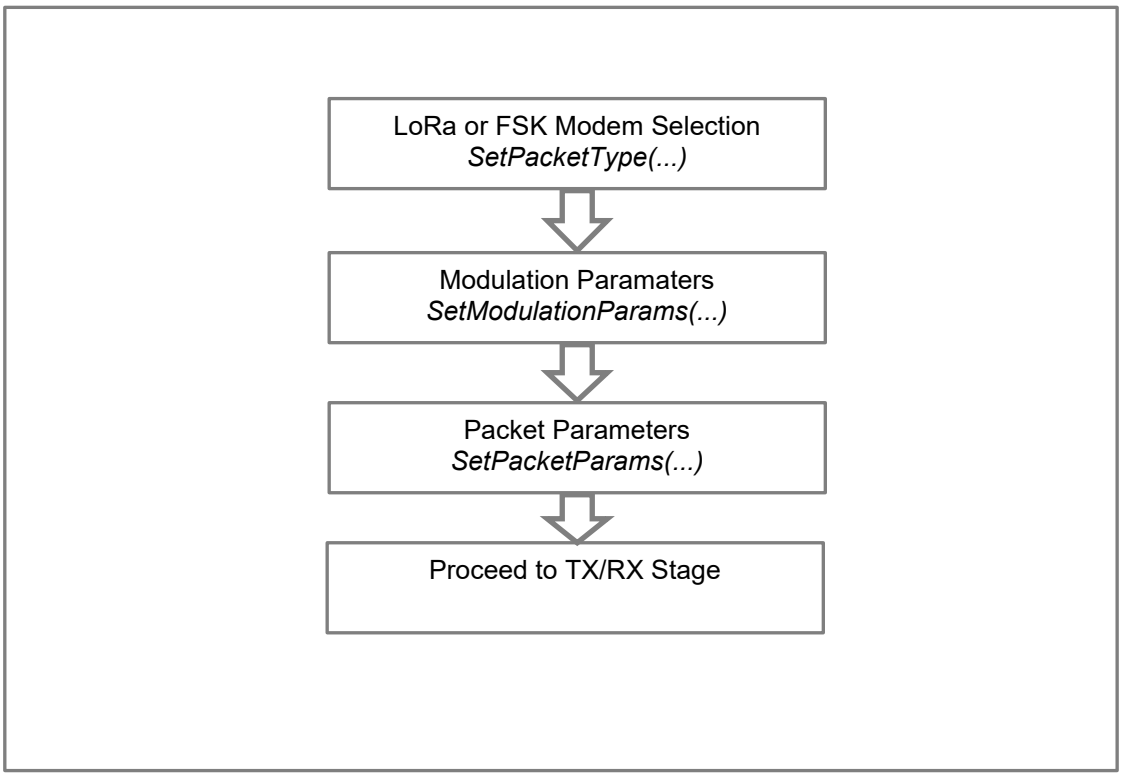


Fig.8 Configuration and Settings - Modem Selection, Modulation and Packet Parameters

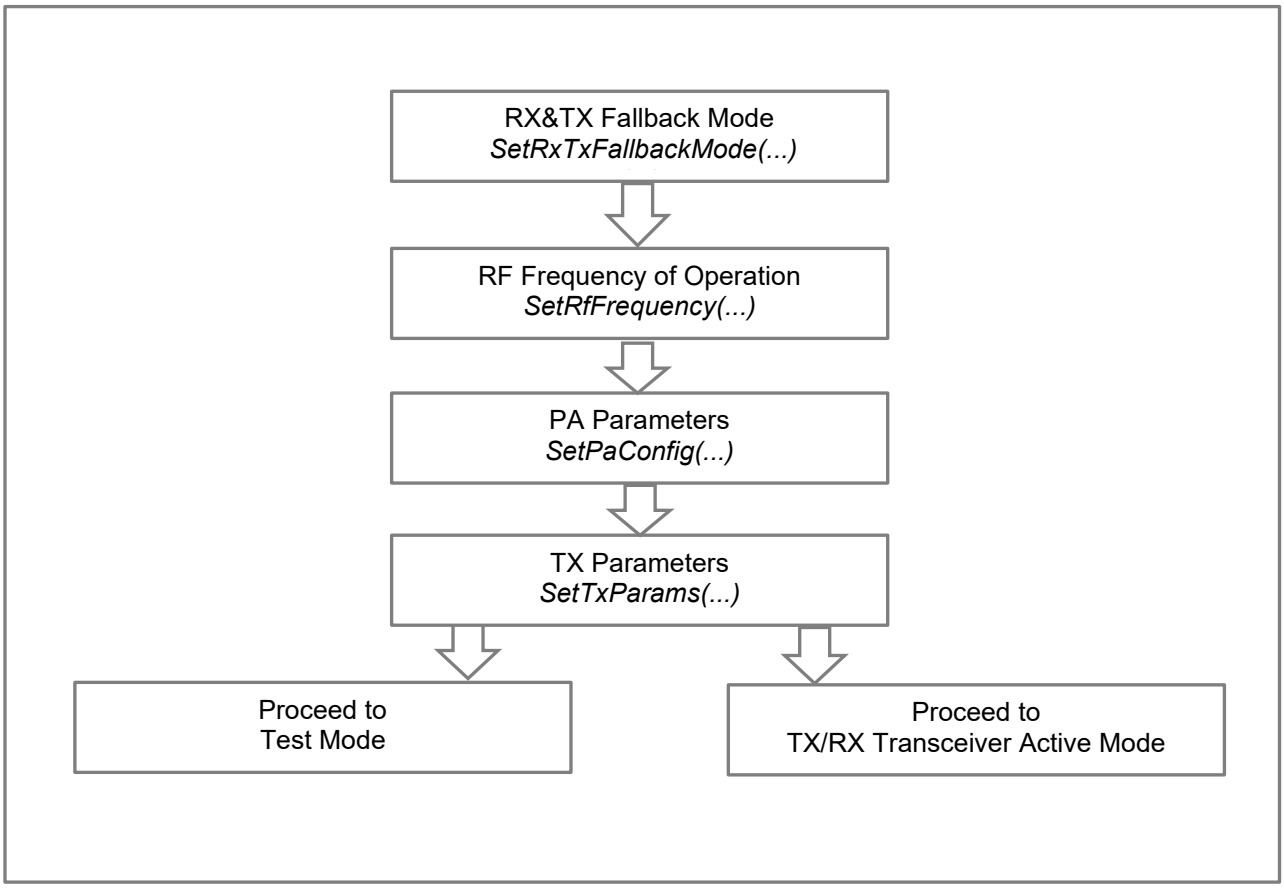


Fig.9 Configuration and Settings – RF Frequency, PA and TX/RX Parameters

7. Drawings

Figure.10 and Figure.11 depict a description of connector pinout and module dimensions for NTR09RFH3/NTR09RSH3 and NTR09CFH3/NTR09CSH3 respectively. A detailed description of the individual pins can be found in Table 22 Connector and Pin Descriptions.

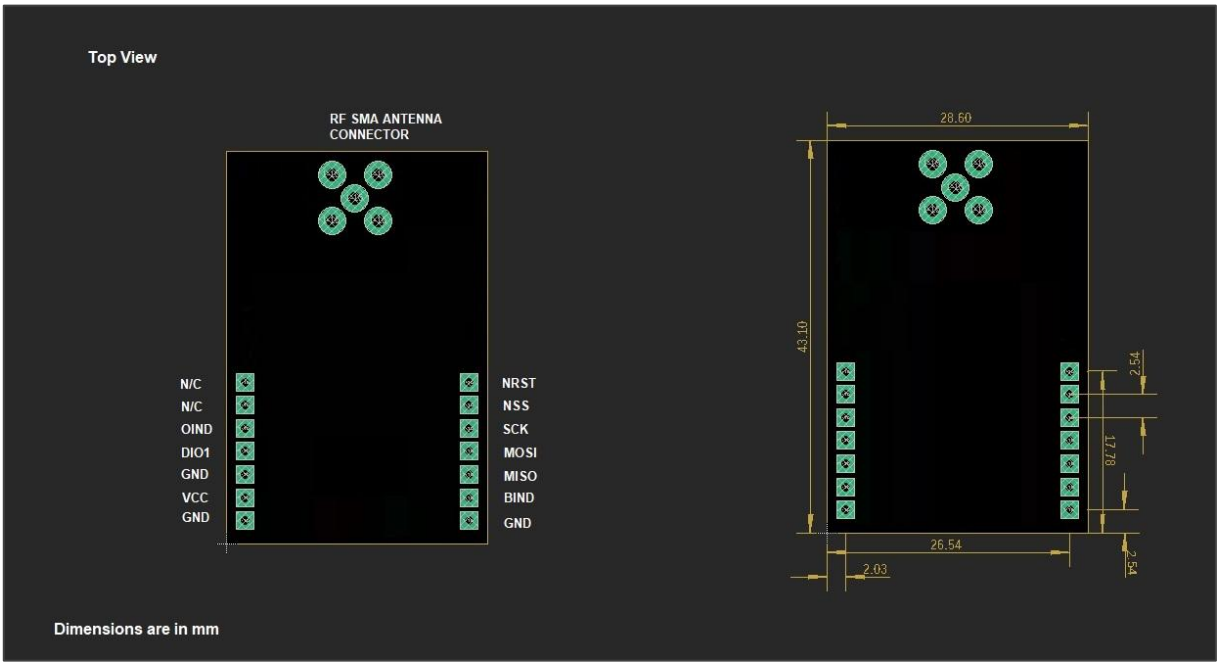


Fig.10 NTR09RFH3/NTR09RSH3 Pin and Size Diagram

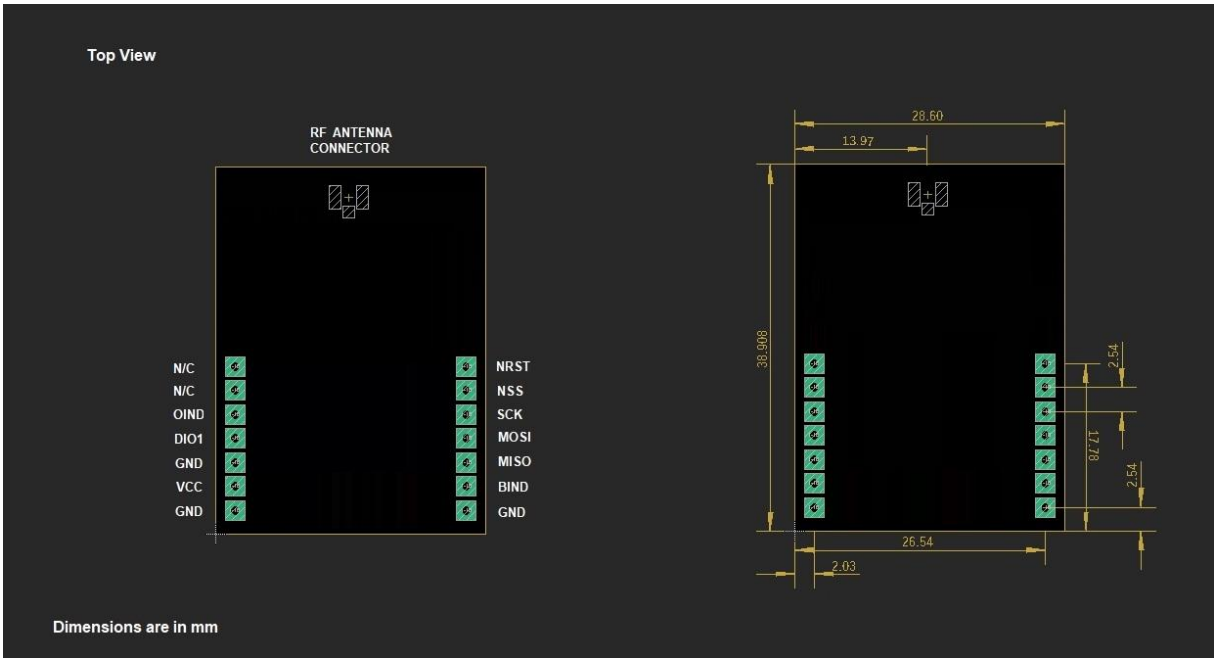


Fig.11 NTR09CFH3/NTR09CSH3 Pin and Size Diagram

CONNECTORS		
Pin No	**Pin Name**	**Pin Function**
CA	ANT	RF Output/Antenna
J1-Connector		
J1-1	N/C	No Connection (Internally GND)
J1-2	N/C	No Connection (Internally GND)
J1-3	OIND	Operation Indicator
J1-4	DIO1	Data I/O
J1-5	GND	0V, Ground
J1-6	VCC	+Supply Voltage
J1-7	GND	0V, Ground
J2-Connector		
J2-1	NRST	Reset
J2-2	NSS	SPI chip select
J2-3	SCK	SPI clock
J2-4	MOSI	SPI MOSI
J2-5	MISO	SPI MISO
J2-6	BIND	Busy Indicator
J2-7	GND	0V, Ground

Table 22. Connector and Pin Descriptions (NTR09RFH3, NTR09RSH3, NTR09CFH3, NTR09CSH3)

8. Ordering Information

Order Code	Description	
NTR09RFH3	NTR09RFH3 315MHz/+20dBm LoRa RF Transceiver Module (with SMA RF Connector)	
NTR09CFH3	NTR09CFH3 315MHz/+20dBm LoRa RF Transceiver Module (with U.FL RF Connector)	
NTR09RSH3	NTR09RSH3 315MHz/+20dBm LoRa RF Transceiver Module (with RF Shield and SMA RF Connector)	
NTR09CSH3	NTR09CSH3 315MHz/+20dBm LoRa RF Transceiver Module (with RF Shield and U.FL RF Connector)	

Table 23. NTR09XXH3 Variants and Ordering Info

Revision History

Date	Revision	Modifications
March 12, 2024	1.1	Initial release

References

1) Semtech SX1262 Datasheet - https://www.egn-elektronik.com.tr/EN/Datasheets/SX1262.pdf

2) SX1262 Drivers - https://github.com/Lora-net/sx126x_driver